

MOS FIELD EFFECT TRANSISTOR 2SK3755

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3755 is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|-------------|-----------------|
| 2SK3755 | Isolated TO-220 |

FEATURES

• Super low on-state resistance

 $R_{DS(on)1} = 12 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 23 \text{ A})$

 $R_{DS(on)2}$ = 18 m Ω MAX. (VGS = 4.5 V, ID = 23 A)

- Low Ciss: Ciss = 1200 pF TYP.
- Built-in gate protection diode

(Isolated TO-220)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

| Drain to Source Voltage (V _{GS} = 0 V) | VDSS | 40 | V |
|---|-----------------------|-------------|----|
| Gate to Source Voltage (VDS = 0 V) | Vgss | ±20 | V |
| Drain Current (DC) (Tc = 25°C) | ID(DC) | ±45 | Α |
| Drain Current (pulse) Note1 | I _{D(pulse)} | ±140 | Α |
| Total Power Dissipation (Tc = 25°C) | P _{T1} | 24 | W |
| Total Power Dissipation (T _A = 25°C) | P _{T2} | 2.0 | W |
| Channel Temperature | Tch | 150 | °C |
| Storage Temperature | Tstg | -55 to +150 | °C |
| Single Avalanche Current Note2 | las | 23 | Α |
| Single Avalanche Energy Note2 | Eas | 53 | mJ |
| Repetitive Avalanche Energy Note3 | Ear | 53 | mJ |

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- 2. Starting T_{ch} = 25°C, V_{DD} = 20 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V
- **3.** IAR ≤ 23 A, Tch $\leq 150^{\circ}$ C

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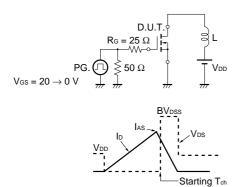


ELECTRICAL CHARACTERISTICS (TA = 25°C)

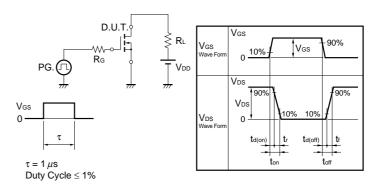
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|----------------------|--|------|------|------|------|
| Zero Gate Voltage Drain Current | IDSS | V _{DS} = 40 V, V _{GS} = 0 V | | | 10 | μΑ |
| Gate Leakage Current | Igss | V _{GS} = ±20 V, V _{DS} = 0 V | | | ±10 | μΑ |
| Gate Cut-off Voltage | V _{GS(off)} | V _{DS} = 10 V, I _D = 1 mA | 1.5 | 2.0 | 2.5 | V |
| Forward Transfer Admittance Note | y fs | V _{DS} = 10 V, I _D = 23 A | 12 | 25 | | S |
| Drain to Source On-state Resistance Note | R _{DS(on)1} | V _{GS} = 10 V, I _D = 23 A | | 9.7 | 12 | mΩ |
| | R _{DS(on)2} | V _{GS} = 4.5 V, I _D = 23 A | | 12.9 | 18 | mΩ |
| Input Capacitance | Ciss | V _{DS} = 10 V | | 1200 | | pF |
| Output Capacitance | Coss | V _{GS} = 0 V | | 330 | | pF |
| Reverse Transfer Capacitance | Crss | f = 1 MHz | | 120 | | pF |
| Turn-on Delay Time | t _{d(on)} | V _{DD} = 20 V, I _D = 23 A | | 10 | | ns |
| Rise Time | tr | V _{GS} = 10 V | | 4 | | ns |
| Turn-off Delay Time | t _{d(off)} | R _G = 0 Ω | | 35 | | ns |
| Fall Time | tf | | | 5 | | ns |
| Total Gate Charge | Q _G | V _{DD} = 32 V | | 25.5 | | nC |
| Gate to Source Charge | Qgs | V _{GS} = 10 V | | 4.2 | | nC |
| Gate to Drain Charge | Q _{GD} | I _D = 45 A | | 7.1 | | nC |
| Body Diode Forward Voltage Note | V _{F(S-D)} | I _F = 45 A, V _{GS} = 0 V | | 0.98 | 1.5 | V |
| Reverse Recovery Time | trr | I _F = 45 A, V _{GS} = 0 V | | 29 | | ns |
| Reverse Recovery Charge | Qrr | di/dt = 100 A/μs | | 30 | | nC |

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



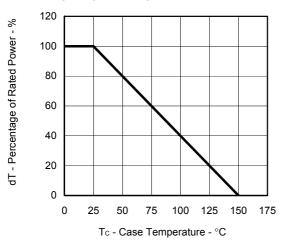
TEST CIRCUIT 2 SWITCHING TIME



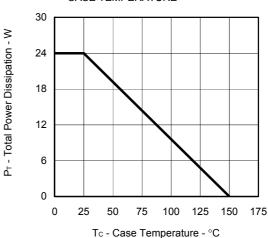
TEST CIRCUIT 3 GATE CHARGE

TYPICAL CHARACTERISTICS (TA = 25°C)

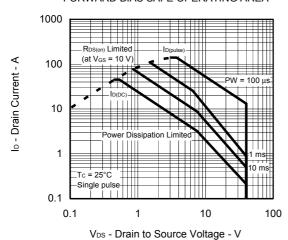
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



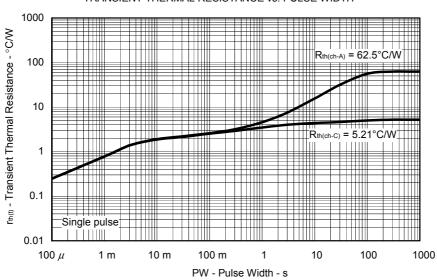
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



lo - Drain Current - A

80

60

40

20

0

0

DRAIN TO SOURCE VOLTAGE 160 140 120 100

1

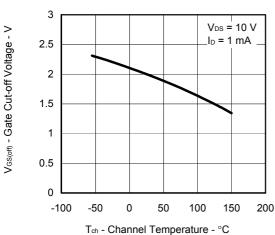
DRAIN CURRENT vs.

V_{DS} - Drain to Source Voltage - V

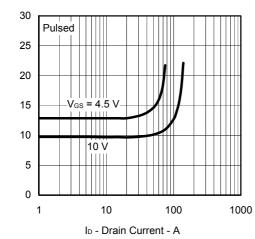
2

3

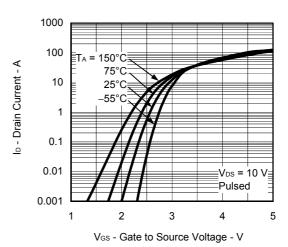




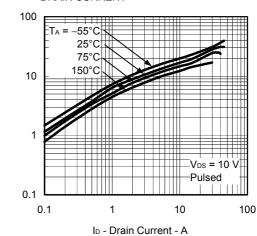
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



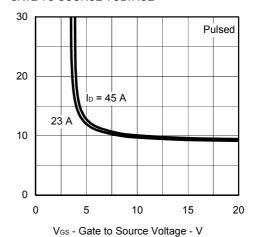
FORWARD TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



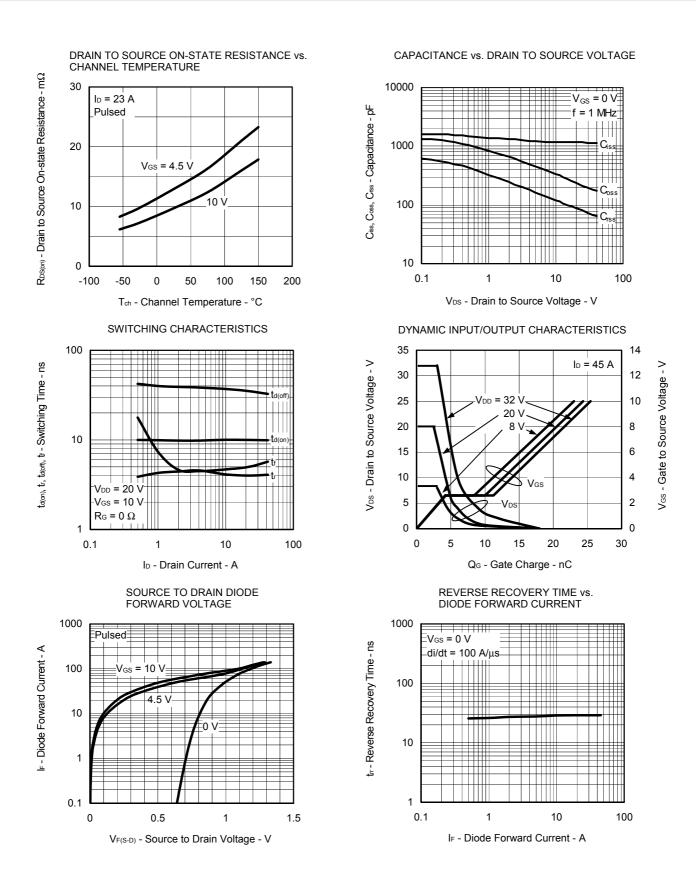
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



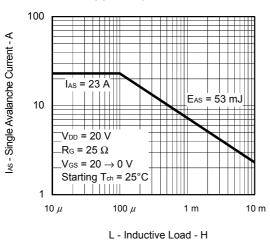
R_{DS(m)} - Drain to Source On-state Resistance - mΩ

l y_s | - Forward Transfer Admittance

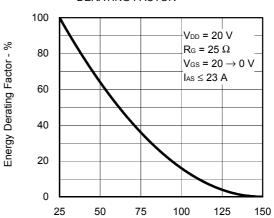
R_{DS(ση)} - Drain to Source On-state Resistance - mΩ



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

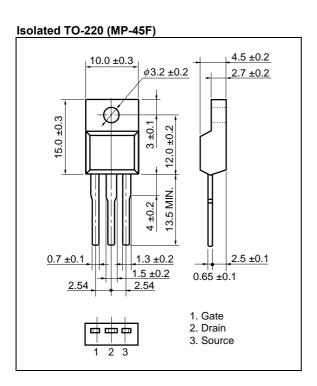


SINGLE AVALANCHE ENERGY DERATING FACTOR

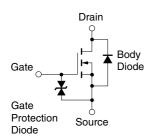


Starting T_{ch} - Starting Channel Temperature - $^{\circ}\text{C}$

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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